REMARKS

Claims 1-8 and 11-20 are pending and at issue. Claims 1-4, 6-8, 11-17, and 19-20 stand rejected as anticipated by Girson et al. (U.S. Patent No. 7,111,179). The remaining claims each stand rejected under a proposed combination of Girson et al. and Choi et al. (U.S. Patent No. 6,233,690). Claim 9 was previously canceled. Independent claims 1 and 13 are amended to recite the limitations of previously entered claims 10 and 21, respectively. Claims 10 and 21 are accordingly canceled. In light of the following remarks, Applicant respectfully asserts that the relied upon art does not teach or suggest the recited subject matter.

Applicant respectfully traverses the rejection of claims 1-4, 6-8, 11-17 as anticipated by Girson et al. Independent claims 1 and 13 are amended to recite obtaining thread runtime performance data including an instructions per clock cycle metric _and_ a memory references-per-clock-cycle metric, and adjusting an operating voltage or an operating frequency of the machine based on the performance data. Girson et al. does not disclose adjusting an operating voltage or an operating frequency based on a memory references-per-cycle metric in any manner, nor is Girson et al. cited for this purpose. Therefore, Girson does not anticipate claims 1-4, 6-8, 11-17.

Applicant respectfully traverses the rejection of any of the pending claims as obvious over Girson et al. in view of Choi et al. Each of the pending claims now recites adjusting an operating voltage or an operating frequency based on a memory references-per-cycle metric as well as an instructions per cycle metric. As discussed above, Girson et al. does not disclose adjusting an operating voltage or an operating frequency based on a memory references-per-cycle metric.

While Choi et al. discloses determining whether a particular processor instruction requires loading data that may cause a predictable wait time, Choi et al. does not disclose determining a memory references-per-cycle metric. Generally, Choi et al. operates to gate (or decouple) a clock signal to a processor based on certain triggers. One such trigger (referenced by the office action) refers to an interlock condition caused by an instruction that locks data from memory as it loads the data, where the termination of the load operating may be estimated based on a data return signal (See Col. 3, lines 20-21) that precedes the load

7

termination by an predictable interval. Upon triggering this interlock instruction type, the Choi et al. system will decouple the clock signal to the processor to reduce power consumption. As discussed during the Examiner interview, a memory reference-per-cycle metric is a rate. Choi et al. does not teach a rate of memory access. Instead, Choi et al. discloses determining if a particular instruction (interlock data access) is being executed and gating clock signals in response thereof. Choi et al. does not disclose or otherwise teach measuring a rate of memory referencing, much less a memory reference-per-cycle metric. Because neither Girson et al. nor Choi et al. disclose adjusting an operating voltage or an operating frequency based on memory references-per-cycle metric as well as an instructions per cycle metric, no combination of Girson et al. and Choi et al. renders the pending claims obvious.
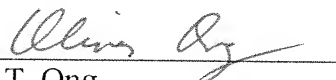
CONCLUSION

For the foregoing reasons, Applicant respectfully requests reconsideration and withdrawal of the rejections/objections and allowance of claims 1-8 and 11-20.

A petition for two-month extension of time is submitted with this response with the appropriate fee. The Commissioner is authorized to charge any fee deficiency required by this paper, or credit any overpayment, to Deposit Account No. 13-2855.

If there are matters that can be discussed by telephone to further the prosecution of this application, Applicant respectfully requests that the Examiner call its attorney at the number listed below.

Dated: May 28, 2008   Respectfully submitted,

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8